BUILT-IN SELF-TESTING FOR DOUBLE DATA RATE INPUT/OUTPUT

ABSTRACT

Macro cells for a Double Data Rate (DDR) I/O interface are provided. The macro cells feature built-in self-test (BIST) functionality for testing the I/O interface at speed, without using external test or evaluation equipment. Each input or output macro cell is configured to generate test signals that are submitted to and processed by the I/O interface. The test signals are then dynamically compared to the signals produced by the interface in response to the test signals and a result is generated. The result may comprise an error signal if the test and response signals do not correspond. An I/O BIST controller may be employed to control the initiation and operation of the macro cells' self-testing.